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Design/Process Checklist for Vehicle Electronic Systems

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400 COMMONWEALTH DRIVE, WARRENDALE, PA 15096

HIGHWAY VEHICLE REPORT

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DESIGN/PROCESS CHECKLIST FOR VEHICLE ELECTRONIC SYSTEMS

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1. INTRODUCTION:

To obtain a high degree of quality and reliability, a wide variety of subjects need to be addressed when designing a vehicle electronic system. No single designer can be expected to have the experience necessary to consider all aspects of a design. Such experience is often spread throughout an organization and not concentrated on any one project.

2. PURPOSE:

The main purpose of this checklist is to provide a systematic approach to insuring that all aspects of an electronic systems design are addressed. Such a list would be useful for design reviews, "fresh eyes" reviews and for education/training.

3. SCOPE:

The following subjects reflect the automotive environment and are based on good engineering practices and past ("lessons learned") experiences. Since it is impossible to be all inclusive and cover every aspect of quality and reliability, this document should be used as a guide for preparation of a checklist that reflects the accumulated "lessons learned" at a particular company.

4. FORMAT:

To keep in a form that will be readily used, each subject will be addressed in an abbreviated format using short, direct, to-the-point phrases. It is not the intent of this document to give a lot of detail, only to point out those subjects that need to be investigated and acted upon.

5. DESIGN CHECKLIST:

5.1 Component Selection/Application: One of the first major concerns for a reliable design is part selection and application. Efforts to use best-in-class suppliers cannot be overemphasized. Much of the input for this topic will come from the corporate electronic components department.

References: 11, 12, 18, 19, 20, 21, 22, data bases of Reliability Analysis Center of IIT Research Institute.

___ Resistors: types, tolerances, packages, reliability concerns, failure modes (for example, opens most common), power/temperature derating.

___ Capacitors: types, tolerances, packages, reliability concerns, failure modes (for example, shorts, value change most common), power/temperature derating.

___ Transistors/Diodes: types, packages, reliability concerns, failure modes, voltage/current/temperature derating.

5.1 (Continued):

___ I.C.'s: types, packages, reliability concerns, failure modes, voltage/current/temperature derating.

___ I.C. Sockets: types, reliability concerns, failure modes.

___ Connectors/Interconnects:

. Types, reliability concerns, failure modes.

.. Between PCB's (for example, individual wires, flat cable, flex cable).

.. Pin/socket connector to wiring harness.

.. Blade/socket connector to wiring harness.

.. Stress relief.

. "Dry" circuits - low voltage, film buildup.

___ Printed Circuit Boards (PCB's):

. Reliability concerns, failure modes.

.. Opens, shorts, warpage.

.. Edge connector (if applicable) to wiring harness - reliability subject to many parameters, for example, plating uniformity, tolerances.

. Material selection.

. Copper thickness (1, 2, and 3 oz).

. Tolerances.

. Thermal considerations (that is, matching of thermal expansions).

. Manufacturability criteria (see section 6).

. EMC criteria (see 5.7.7).

___ Thick film substrates:

. Reliability concerns, failure modes.

. Material selection.

. Tolerances.

5.1 (Continued):

- Thermal considerations (that is, matching of thermal expansions).
- Manufacturability criteria (see section 6).
- EMC criteria (see 5.7.7).

___ Potting, conformal coating: where used, types, limitations.

___ Identification of critical reliability components: for example, power transistors, power zeners, etc.

___ Special requirements for these critical components: derating, screening, handling, failure mode response.

___ Components to avoid: for example, variable resistors if fixed can be used, hand inserted parts if auto insertion viable.

___ Part availability.

___ Part specifications: for example, MIL-STD-883, MIL-STD-202.

___ Testing sample size: statistical significance, attribute or variable data, cost/time/test facility limitations.

___ Electrostatic Discharge: most sensitive components, precautions, handling.

___ Vendor quality/reliability control program.

___ Acceptable Quality Level (AQL), in parts/million (ppm), required: how verified.

___ Process flow/control plans.

___ Process change procedures.

___ Closed loop failure analysis, corrective action plan.

___ Degree of component Statistical Process Control (SPC) used: where used, adherence, effect on AQL.

5.2 <u>Thermal Considerations (Components/Assemblies)</u>: Temperature has a major effect on reliability. In fact, as the temperature of a system rises, thermal failures almost completely overweigh failures from other causes.

References, 3, 11, 12, 13, 14, 15, 16, 17, 22.

5.2 (Continued):

___ Conduct thermal survey of environment (under hood, passenger compartment, etc.): start temperature (heat, cold soak), warm up time, operational temperature (range, rate of temperature change, frequency of change), number of cycles, cooling effects.

___ Assembly (module) temperature environment vs. reliability: field experiences.

___ Component (resistor, capacitor, transistor, diode, etc) thermal analysis: worst case analysis (electrical loading, environment), heat sinking, derating (safety margins).

___ Assembly (module) thermal analysis: worst case analysis (electrical loading, environment), heat sinking, derating (safety margins).

___ Thermal analysis using thermal resistance values is best case: does not consider non linearity (hot spots), interface bonds <100% of area.

___ Thermal testing evaluation: for example, thermocouple critical areas in module and test under worst case electrical loading and environment in temperature chamber. Vehicle evaluation shall also be done (temperature chamber, wind tunnel, etc).

___ Different expansion coefficient stresses: potting, conformal coating, Surface Mount Devices (SMD's), Leadless Chip Carriers (LCC's), PCB interfaces, etc.

___ Rules for mounting components.

___ Rules for mounting assemblies (modules).

___ Thermal shock (splash, cold start): typical failure modes.

___ Identification of critical components and special requirements.

___ Thermal stress test for design verification: tailored to find defects in new design, should be failure oriented (overstressed). Temperature cycling profile: extremes, number of cycles, rate of change, when powered, parameters monitored.

___ Thermal stress test for qualification: mission life oriented. Temperature cycling profile: extremes, number of cycles, rate of change, when powered, parameters monitored.

___ Thermal stress test for production acceptance: should include Environmental Stress Screening (ESS) tailored to reduce infant mortality and precipitate process problems. Temperature cycling profile: extremes, number of cycles, rate of change when powered, parameters monitored.

5.2 (Continued):

___ Combined thermal stress with other tests (for example, thermal, vibration, humidity, voltage) more realistic.

___ Testing sample size: statistical significance, attribute or variable data, cost/time/test facility limitations.

5.3 Vibration/Shock Considerations (Components/Assemblies):

References: 3, 11, 13, 14, 16, 17, 22.

___ Conduct vibration/shock survey of environment (under hood, passenger compartment, etc.): conditions (bumps/potholes, road vibration, handling, rail shock), type (sine, random, complex), frequency range, amplitude/Power Spectral Density (PSD), axis, duration.

___ Stresses on components, bonds, mounting brackets, etc.: concerns, typical failure modes.

___ Rules for mounting components: for example, part size/mass vs. mounting technique.

___ Module mounting techniques: consider mounting bracket effects (for example, resonances).

___ Resonances: conduct resonant search, failure modes, solutions.

___ Vibration test for design verification: tailored to find defects in new design, should be failure oriented (overstressed). Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.

___ Vibration test for qualification: mission life oriented. Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.

___ Vibration test for production acceptance: should include Environmental Stress Screening (ESS) tailored to reduce infant mortality and precipitate process problems. Type (sine, random, complex), frequency range, amplitude/PSD, axis, duration, monitored to detect intermittents.

___ Shock test for design verification, qualification and production acceptance: similar to vibration above.

___ Conduct vibration/shock testing before climatic testing (if done separately).

___ Vibration/shock combined with temperature cycling, humidity more realistic.

___ Testing sample size: statistical significance, attribute or variable data, cost/time/test facility limitations.

5.4 Humidity/Splash/Dust Considerations (Components/Assemblies):

References: 3, 11, 13, 14, 22.

___ Component/Assembly sealing: gasketing, potting, etc.

___ Connector integrity: type of connector (open, sealed, greased, etc).

___ Failure modes: shunt resistance, series impedance.

___ Test procedure for design verification: similar to 5.2, 5.3.

___ Test procedure for qualification: similar to 5.2, 5.3.

___ Test procedure for production acceptance: similar to 5.2, 5.3.

___ More realistic if combined with temperature cycling, vibration.

___ Testing sample size: statistical significance, attribute or variable data, cost/time/test facility limitations.

5.5 Burn In:

___ Determine need, component vs. assembly or both: field correlation, experiences, cost analysis.

___ Component burn-in: which ones, more stress than assembly, minimizes rework. If ppm failure rates low, burn-in may make worse (handling, ESD).

___ Assembly burn-in: thermal mass test considerations.

___ Test conditions: elevated temperature and voltage accelerates failure modes (different times for different failure modes). Static, dynamic operation.

___ Determine optimum burn-in empirically: time vs. temperature/voltage failure rates.

___ Combined powered thermal cycle and burn-in.

___ Testing sample size: statistical significance, attribute or variable data, cost/time/test facility limitations.

5.6 Electromagnetic Compatibility (EMC):

References: 1, 2, 4, 5, 6, 7, 8, 9, 10, 22, 23, 24.

5.6.1 <u>Component Level</u>:

___ Radiated Susceptibility:

. Moderate Radio Frequencies (RF) fields (50 volts/meter): represents nearby transmitters, low power on-board transmitters.

. High RF fields (100 volts/meter): represents high power (100 watt) on-board transmitters.

. Test procedures: SAE J1113, SAE J1448, and SAE J1547.

___ Radiated Emissions:

. On board entertainment/communications antennas and radio sensitivities determine specification limit.

. Test procedures: MIL-STD-461.

___ Conducted Susceptibility:

. Supply Voltage:

.. Normally 10 to 16 V.

.. Reverse battery.

.. Overvoltage: failed regulator (17 V), double voltage jump start.

.. Cold start: 5 to 6 V.

.. Ignition switch rotation: voltage dropouts.

. Vehicle electrical system noise (for example, load dump, switch arcing, inductive transients).

. Test procedure: SAE J1113.

___ Conducted Emissions: Test procedure: VDE 0879, part 3.

___ Electrostatic Discharge (ESD):

. ±15 kV.

. Test procedure: SAE J1113, SAE J1595.

5.6.2 Vehicle Level:

___ Vehicle EMC test procedures.

. Internally generated EMI: check interactions of subsystems under various conditions.

. Radiated susceptibility: 10 kHz to 1 GHz or higher, powerlines, nearby lightning: SAE J1338, SAE J1507, SAE J1407.

. Radiated emissions: SAE J551, SAE J1816.

. ESD: SAE J1595.

. Charging system anomalies: disconnected battery (engine running), load dump, malfunctioning regulator, reverse battery.

5.7 Circuit Design Guidelines:

References: 12, 15, 22.

5.7.1 General:

___ Minimize number of parts.

___ Maximize use of proven circuits.

___ Maximize use of standard parts and widest tolerances.

___ Use slowest speed technology consistent with function.

___ Where possible, include hysteresis on analog/digital circuits.

___ High gain circuits with differential inputs (for example, op-amps, comparators) should use filter capacitor across inputs and/or capacitor from each input to ground.

___ Breadboards may aggravate problems: long leads, poor ground(s).

___ Discrete vs. custom circuits: cost, reliability, volume tradeoffs. For custom circuits, use pessimistic cost/timing.

___ Redundancy: critical circuits.

___ Designed for manufacturability: see process guidelines section 6.

___ Repairability, remanufacturing (if applicable), rework considerations.

___ Diagnostics considered in design.

5.7.1 (Continued):

___ Terminate unused inputs to I.C.'s.

___ Relay precautions: for example, diode increases dropout time, contact arcing, transients, contact sticking.

5.7.2 Components - Specific Devices:

___ Transistors/Diodes/MOSFET's:

. Consider diode/zener response time to transients.

. Transistor within safe operating area (SOA). Consider temperature, loading, signal input.

. Use transistor base to emitter resistor.

. Collector to housing stray capacitance for switching circuits: may cause radiated emissions.

. Limit base/gate drive: fast drive into saturation creates noise, balance Electromagnetic Interference (EMI) with heat dissipation.

. MOSFET's: ESD one of major failure modes.

___ Linear (Op Amps, etc):

. Consider single supply limitations: input range usually does not include power supply rails, output loading determines voltage range.

. Overdriven inputs: may drive output to power supply rail (transmits power supply noise).

. High gain amplifiers: stability, oscillations, stray capacitance and inductance varies with temperature/sample.

. Use Bode gain/phase plot analysis to determine stability margin.

. Differential amps: consider all sources of unbalance to ground, DC and AC (for example, capacitors, source impedance).

. Differential amps limited in rejection of common mode signals at higher frequencies.

. Use op amp internal compensation capacitor, if accessible, for filtering (acts as nonlinear filter).

. Voltage follower latch up: input levels too high.

5.7.2 (Continued):

. Avoid high impedances.

___ Digital (microprocessors, etc.):

. Fanout limitations: for example, loading affects propagation delays especially for CMOS.

. Logic levels compatible over minimum and maximum temperature/specification limits.

. Maximize logic levels margins (for example, V low max and V high min).

. CMOS: latchup when input > power supply or < ground.

. Microprocessor clock: operates, including start up, under all temperature and power supply transitions.

5.7.3 <u>Module Inputs</u>:

___ Protection for shorts to ground/power.

___ Switch requirements: contact material/pressure, type of connector, minimum voltage/current for oxidation burn through (dry circuits).

___ Allow for contact resistance, shunt resistance.

___ Maximize input thresholds for noise immunity.

___ Maximize input filtering considering maximum signal information delay, minimum signal pulse width to be recognized, fastest signal rate of change (dV/dT).

___ Shared sensors compatible: that is, one sensor to multiple modules.

5.7.4 <u>Module Outputs</u>:

___ Protection for shorts to ground/power.

___ Inductive driver transient protection.

___ Output driver current source vs. current sink considerations: current source has same failure mode (wiring short or open).

___ Limit high current actuator transition times (without overheating): generates noise, wiring harness ringing.

___ H-Bridge driver: insure both drivers in each leg not on simultaneously during transitions.

5.7.5 Power Supply Related:

___ Circuits compatible with run - start - run cycle (starting) et al.

___ Power up/down sequence

___ Overvoltage, undervoltage, reverse voltage, load dump.

___ Power supply protection schemes.

___ Power supply regulator response time: not too fast or may be noise sensitive.

___ Power supply capacitor design: for example, aluminum electrolytic voltage/temperature, ripple calculations.

___ Avoid voltage divider circuits. If used, use worst case power supply voltages.

___ Minimum current draw may deregulate power supply.

___ Two power supplies may cause latch up if not tracking.

___ For mixed technologies (for example, CMOS, TTL), power up/down may produce errors due to different valid/invalid levels.

5.7.6 Electrical Overstress:

___ Ignition arcover design considerations for under hood applications.

___ Transient protection: Resistor, Capacitor, R/C, clamps (for example, zener, diode).

___ All circuits connected to main power, or through loads to main power, must withstand electrical overstress.

___ Shutdown circuits must have fast response.

___ ESD protection:

. Often misanalyzed as electrical overstress.

. Part (for example, IC) protection limited: too slow (ESD <5 ns.).

. Use Resistor, Capacitor, R/C, clamps: consider high peak voltage.

5.7.7 PCB layout rules for EMC:

___ Ground plane interconnecting circuit grounds: ideally greater than 50% of PCB area.

___ Common impedance: sensitive circuits not shared with high rate of current change (dI/dT) circuits. E = L * dI/dT (typically, L = 25 nh/in).

___ Decoupling capacitors very near IC's, especially microprocessors and high dI/dT circuits. Use ground plane between capacitor and IC ground.

___ Input/output filtering configurations: near entry of Input/Output, grounded via ground plane.

5.7.8 Circuit Tolerance/Analysis:

___ Sneak circuit analysis.

___ Failure Modes and Effects, criticality (severity/probability) analysis.

___ AQL for assembly (module) levels required, how determined.

___ Reliability Prediction models used for assembly:

. MIL-STD-217: not directly applicable, assumes exponential failure distribution (no infant mortality). Need automotive data base. Consider dormancy.

. Field experience: reliability growth model. Similar equipment, complexity/function.

___ Degree of circuit/tolerance analysis used:

. Worst case combinations of part tolerances/inputs over temp. range.

. Design of Experiments, Taguchi methods.

. Monte Carlo method.

. Component aging considered: value change with stress, time.

5.8 Software:

___ Use modularization.

___ Optimize decoupling with other software modules.

___ Designed for testability.

5.8 (Continued):

___ Documentation.

___ Sufficient time allowed for testing and debug: can be as much as design and coding.

___ Software module testing: simulation on mainframe.

___ Static (change inputs manually) bench testing of system (total program).

___ Dynamic (many combinations of inputs) design verification on mainframe simulator.

___ Fault tolerance: for example, inputs within realistic limits (for example, dV/dT, dFreq./dT, edges, change in A/D counts).

___ Watchdog timer strategy and implementation.

___ Low voltage reset.

___ Fault tolerance strategy: revert to old data, ignore, try again.

___ Software noise immunity strategies and limitations.

___ Switch contact bounce strategy.

___ Software development tools: portable engineering and calibration consoles.

___ Vehicle testing program.

5.9 <u>Diagnostics</u>:

___ What functions to check: assign probability/severity index.

___ Diagnostic troubleshooting procedures: philosophy, documentation.

___ Diagnostics considered in warranty analysis.

___ Built in monitor circuits.

___ Warning indicators: for example, instrument panel light.

___ Intermittents: how to precipitate, store in nonvolatile memory.

___ Self Test Methodology: factory and field service.

5.9 (Continued):

___ Test equipment requirements.

___ Software memory allocation.

5.10 Miscellaneous Design Guidelines:

___ Identify critical characteristics from customer perspective: Quality Functional Deployment (QFD).

___ Vehicle wiring guidelines:

. Critical modules that must operate during engine cranking (for example, electronic engine controls) may require power and ground feeds directly to battery (minimizes common impedance, voltage drops).

. Low level signals: do not use sheet metal return.

. Maintain low resistance between body panels/structures.

. Avoid unterminated wires: acts as antenna.

. Sensitive wiring >5 cm from secondary ignition parts (for example, ignition wires, coil, plugs, distributor).

. Test for wiring crosscoupling and correct (separation, twisting, etc).

. Twisted wires: effective low cost option for noise reduction.

. Wire shielding: verify need (usually needed for wire crosscoupling), insure coverage in area of noise, single point ground (drain wire short).

. Maximize wire routing near sheet metal.

. Analyze multiple grounds: ground loops.

. Inductive loads: test for noise and if excessive suppress.

. Insure reliability of ground connections to sheet metal.

. Ignition arcover: maintain separation, "non conductors" may be conductive (for example, carbon loaded hoses, wet plastic).

___ Allow for impedance buildup during system life.

___ Vehicle durability, field testing program.

___ Failure Modes and Effects analysis: module, subsystem, system level.

5.10 (Continued):

___ Criticality analysis (severity/probability of occurence): module, subsystem, system level.

___ Limited operation strategy.

___ Design reviews, audits at various stages.

___ Design change procedures.

___ Closed loop failure analysis and corrective action plan: concern description, define root cause, containment, corrective actions, verification of containment/corrective actions, prevent recurrence.

___ Analyze warranty returns: "non defective returns" often >50% of returns, functional testing at temperature limits often will not identify problem. Use Environmental Stress Screening to precipitate problems.

___ Factor accessibility: harder to replace item within system will have better warranty.

___ Wiring harness reliability affects module warranty.

6. PROCESS CHECKLIST:

The manufacture of electronic components/modules is a process that is continually being changed. These guidelines are basically intended for the module design engineer so that a greater appreciation of what is involved can be obtained and considered in the early design stages.

6.1 Through Hole (TH) Technology:

6.1.1 General TH Design Guidelines:

___ For single sided PCB, conductor width = 0.020 in minimum.

___ For double sided PCB, power/ground conductor width = 0.016 in minimum, signal conductor width = 0.012 in minimum.

___ Plated through hole (PTH) pad diameter = or >2 x hole diameter.

___ PTH diameter = or >40% of material thickness.

___ PTH double sided: hole diameter 0.010 to 0.028 in > lead diameter.

___ PTH single sided: hole diameter 0.005 to 0.020 in > lead diameter.

___ Do not use sharp corners for conductor traces.

___ Web between holes: for punched holes = 0.060 in minimum or 1.5 times hole diameter whichever is greater. For drilled holes = 0.035 in minimum.

6.1.1 (Continued):

___ Warpage: balance copper density within 30% both sides. For large copper areas (for example, ground plane), use voids at random intervals.

___ Use thermal relief around component holes in large copper areas.

___ Auto insertion: hole diameter >0.015 in over lead diameter minimum.

___ Lead formed double kink parts for PTH: euroform type prefered, stress relief, trapped gas in PTH area.

___ For clinched leads, use tear drop pads: more bonding area.

___ Solder mask: types (screened, dry film).

6.1.2 Process Steps:

___ Component packaging: for example, bulk and vibration feeders (avoid both), reel/tape.

___ Parts insertion, clinching: automatic, hand.

___ Wave solder process: types, variables.

___ Solder/flux chemistry.

___ Cleaning: for example, flux residues, solvents, migration.

___ Solder inspection criteria.

___ Potting/conformal coating.

___ Testing/inspection: during assembly, final assembly, automatic, high density concerns.

___ Repair/rework philosophy for PTH technology.

___ SPC: where used, adherence, effect on AQL.

___ ESD practices unique to TH technology.

6.2 Thick Film Hybrid (TFH) Technology:

6.2.1 General TFH Design Guidelines:

___ Resistors: 10 to 200 ppm/C, ±15% tolerance typical (untrimmed). Top hat resistors more susceptible to high voltage arcover.

___ Conductor: paladium silver = 0.035 ohms/square, 0.08 with solder coating, 250 - 800 ppm/C.

___ Conductor signal width/spacing normally 0.5 mm.

6.2.1 (Continued):

___ Component attachment pad configuration.

___ Minimize crossovers and number of resistive paste values.

___ Conductor concerns.

. Silver migration: silver + electrolyte + moisture = dendritic growth of silver (0.020 in gap in minutes with 0.5 V bias). Preventive measures = cleaning, potting.

. Galvanic action: Alum + electrolyte + moisture = battery with paladium or silver (2.5 to 2.8 V). Preventive measures = cleaning, potting.

. Intermetallics: Paladium + tin = poor adhesion of pal silver films (conductor adhesion). Control solder.

6.2.2 <u>Process Steps</u>:

___ Screen/print, fire conductors.

___ Double screen/print, fire dielectric (crossovers).

___ Screen/print, fire resistors.

___ Trim: for example, laser, scribe.

___ Solder screen.

___ Conductive epoxy vs. solder paste.

___ Solder/flux chemistry.

___ Component packaging: for example, bulk and vibration feeders (avoid both), reel/tape.

___ Pick/place components.

___ Reflow solder: variables = component mass, specific heat, furnace set point, belt speed.

___ Cleaning: for example, flux residues, solvents.

___ Solder inspection criteria.

___ Break substrate apart.

___ Wire bonding (if applicable).

. Materials: gold, aluminum (most common).

. Thermocompression.

6.2.2 (Continued):

. Ultrasonic: most common.

. Thermosonic: 0.001 to 0.005 gold wires.

___ Potting/coating.

___ Testing/inspection: during assembly, final assembly, automatic, high density concerns.

___ Repair/rework philosophy for TFH technology.

___ SPC: where used, adherence, effect on AQL.

___ ESD practices unique to TFH technology.

6.3 <u>Surface Mount Device (SMD) Technology</u>: There are three types of SMD technology:

Type 1 - All SMD's
Type 2 - SMD's and/or TH on top, SMD's and/or TH on bottom of PCB
Type 3 - TH on top, SMD's on bottom of PCB.

At this time, Type 3 is most common in the automotive world so it will be used as an example.

6.3.1 <u>General SMD Design Guidelines</u>:

___ See 6.1 for items similar to TH technology.

___ Vias, test pads not part of attachment pad.

___ Lead coplanarity (flatness): <0.004

___ Underside leaded component clearance: >0.010 for solvent action.

___ Component orientation relative to soldering direction.

___ Tombstoning prevention.

6.3.2 <u>Process Steps</u>:

___ Component packaging: for example, bulk and vibration feeders (avoid both), reel/tape.

___ Parts insertion/clinch TH devices.

___ Flip PCB.

___ Apply adhesive: type, concerns.

6.3.2 (Continued):

___ SMD component packaging: for example, bulk, and vibration feeders (avoid both) reel/tape.

___ Place SMD's.

___ Cure adhesive.

___ Flip PCB.

___ Wave solder process.

___ Solder/flux chemistry.

___ Cleaning: for example, flux residues, solvents, migration.

___ Solder inspection criteria.

___ Potting/conformal coating.

___ Testing/inspection: during assembly, final assembly, automatic, high density concerns.

___ Repair/rework philosophy for SMD technology.

___ SPC: where used, adherence, effect on AQL.

___ ESD practices unique to SMD technology

6.4 <u>Miscellaneous Process Guidelines</u>:

___ Design engineer interface with manufacturing throughout project.

___ Conduct feasibility study.

___ Compatibility of parts/tooling: assessed early in design phase.

___ Incoming inspection: vendor quality #1 reliability concern.

___ In-process and end of line test requirements.

___ Repair/rework methods.

___ Layout for EMC: see 5.7.7.

___ Electrostatic discharge (ESD) control program, training.

___ Vision technology: type, where used.

___ Optimize utilization of PCB, TFH area: use standard sizes.